

Serial No. 09/191,629

Reply to Office Action of May 22, 2003

**Amendments to the Specification:**

Please replace the paragraph at page 5, beginning at line 12 with the following:

Referring to Figure 2, a computer system S according to the present invention incorporates a digital television (DTV)/peripheral component interconnect (PCI) interface logic 36. A DTV tuner 37 receives encoded DTV data through an antenna [[87]] 81 and provides the encoded or compressed DTV data to the DTV decoder 35. The DTV decoder 35 decompresses or decodes the DTV data. The DTV/PCI interface logic 36 receives decoded digital television (DTV) data from the DTV decoder 35. The decoded DTV data is pumped over a PCI bus 20 by the DTV/PCI interface logic 36 to a core logic 10. The core logic 10 may include a system memory controller, an integrated accelerated graphics port (AGP), and the PCI bus 20. An example of a suitable core logic 10 is Intel's 440BX chipset. The core logic 10 passes the DTV data across the AGP to a graphics controller 14. An example of a suitable graphics controller is the ATI 3D RAGE LT PRO manufactured by ATI Technologies, Inc. The graphics controller 14 provides DTV data to and retrieves DTV data from a conventional graphics controller frame buffer 28. From the graphics controller 14, outgoing DTV data may be provided to a display screen or other display device 34. The outgoing DTV data is synchronized to the refresh rate of the graphics controller 14. The graphics controller 14 provides DTV data (i.e., RGB data) to the display screen 34. The transfer path for DTV data from the interface logic 36 through the graphics controller 14 is represented by a phantom arrow line 21. The system S eliminates the need for a video port cable and a non-standard graphics controller video port typically used for transfer of analog television data in a conventional computer system. Further, transfer of DTV data in the computer system S is independent of the type of graphics subsystem.